Low Power and Area Efficient 64 Bit Vedic Multiplier Design for High Speed Operation in ASIC-DSP Applications

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Bios

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Motivation

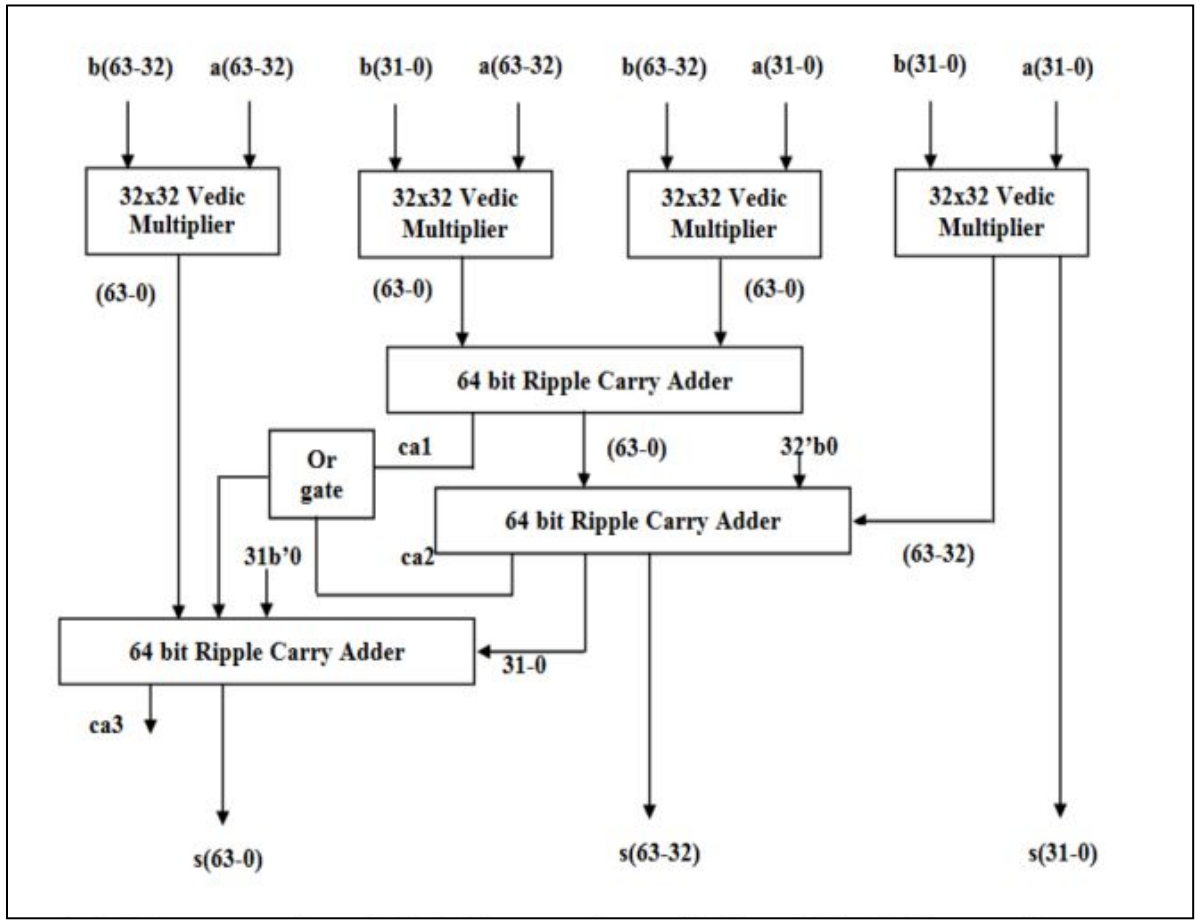
- As we are aware of that all kinds of multipliers are widely applicable in ASIC's and DSP applications. While all the multipliers provide conventional way of multiplying but has high consumption operations.
- Vedic Multiplier is an ideal choice as it is best suitable for low power, reduced computation time as well as reduced area requirement compared to conventional multipliers.
- Vedic Mathematics is very easy for mental as well as manual computations.
- The sutra (algorithm) has lesser operations and has natural inherent consideration to be more efficient.
- Applying the sutra for multiply large 64-bit numbers is easy due to it simplicity in its operation
- Since a multiplier is a basic element for many library components, savings in power and area as well as higher speeds will have cascading effects on IPs, ASICs and DSPs.

Main Idea

- Vedic Multipliers are playing vital role to speed up operations, optimized area and power when compared to standard multipliers.

- It uses Urdhva Tiryakbhyam sutra based algorithm discovered by Scientist Bharati Krishna Tirtha(1884-1960) who is titled as Jagadguru Shankaracharya and written in his book Vedic mathematics. This algorithm uses crosswise and vertical multiplication which gives low power, reduced timing and optimized area (PTA).

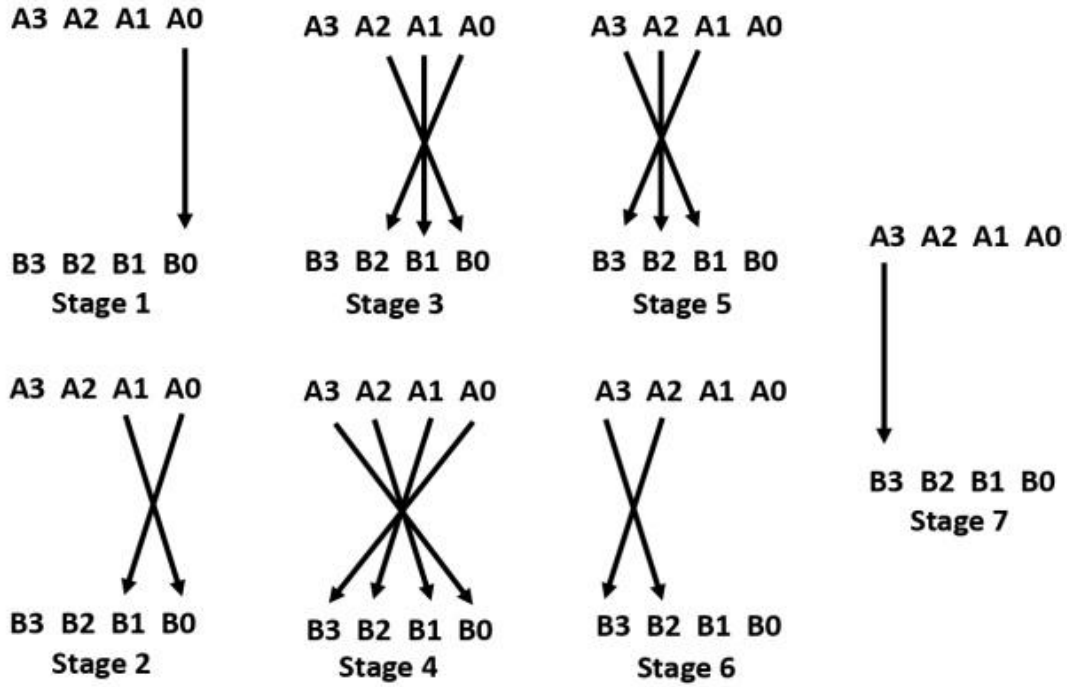
- This work is proposing a native 64-bit multiplier and establishing disruptive new design for basic component like ASICs and DSP which have cascaded effects on all the designs. The strategy is to compare physical design and PTA reports to show that the architecture itself will indicate improved PTA.



Implementation of 64x64 Bit Vedic Multiplier using 32-bit Multipliers

Cont.

- The concept of UT sutra is applied to each binary bits for vertically and crosswise multiplication resulting in an order of increase to the speed of the multiplication and reduce the execution steps. The following demonstrates the steps in the process:



Line diagram for the native Urdhva-Tiryagbhyam algorithm

Stage 1: k0 = A0 B0

Stage 2: k1 = A1 B0 +A0 B1

Stage 3: k2 = A2 B0 +A1 B1 +A0 B2

Stage 4: k3 = A3 B0 +A2 B1 +A1 B2 +A0 B3

Stage 5: k4 = A3 B1 +A2 B2 +A1 B3

Stage 6: k5 = A3 B2 +A2 B3

Stage 7: k6 = A3 B3

The products are obtained by adding S1 S2 S3 where S1 S2 S3 are the partial sums.

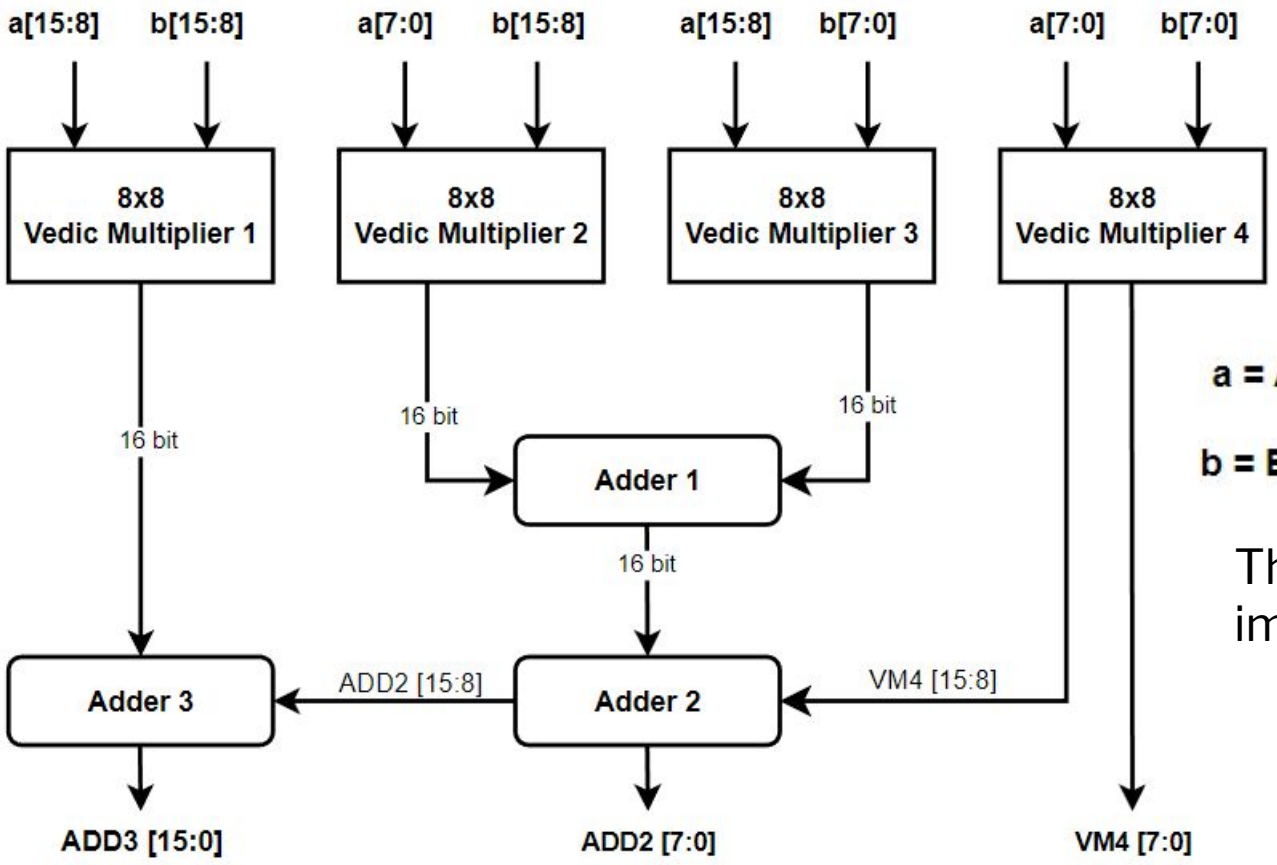
$$S1 = k_6 k_5[0] k_4[0] k_3[0] k_2[0] k_1[0] k_0$$

$$S2 = k_5[1] k_4[1] k_3[1] k_2[1] k_1[1]$$

$$S3 = k_3[2]$$

$$\begin{array}{llllllll} \text{Product} = & k_6 & k_5[0] & k_4[0] & k_3[0] & k_2[0] & k_1[0] & k_0 + \\ & k_5[1] & k_4[1] & k_3[1] & k_2[1] & k_1[1] & 0 & + \\ & & & k_3[2] & 0 & 0 & 0 & \\ \hline P7 & P6 & P5 & P4 & P3 & P2 & P1 & P0 \end{array}$$

Implementation:



Implementation of 16x16 Bit Vedic Multiplier using 8-bit Multipliers

a = A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

b = B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0

The similar concept can be extended to use for implementation of 64-bit Vedic multiplier

Design Implementation

```
    s[0] = {k[14][0],k[13][0],k[12][0],k[11][0],k[10][0],k[9][0],k[8][0],k[7][0],k[6][0],k[5][0],k[4][0],k[3]
[0],k[2][0],k[1][0],k[0][0]};

    s[1] = {1'b0,k[13][1],k[12][1],k[11][1],k[10][1],k[9][1],k[8][1],k[7][1],k[6][1],k[5][1],k[4][1],k[3][1],k[2]
[1],k[1][1],1'b0,1'b0};

    s[2] = {k[7][2],1'b0,1'b0,1'b0,1'b0,1'b0,1'b0,1'b0};

    s[3] = {1'b1,1'b0,1'b0,1'b0,1'b0,1'b0,1'b0,1'b0};

    re[3] = s[0] + s[1] + s[2] ;

    adder[0] = re[1]+re[2];
    adder[1] = adder[0]+re[3][15:8];
    adder[2] = re[0]+adder[1][15:8];

    product = {adder[2],adder[1][7:0],re[3][7:0]};
    $display("Product = %b(%0d)",product,product);
```

Source Code Logic

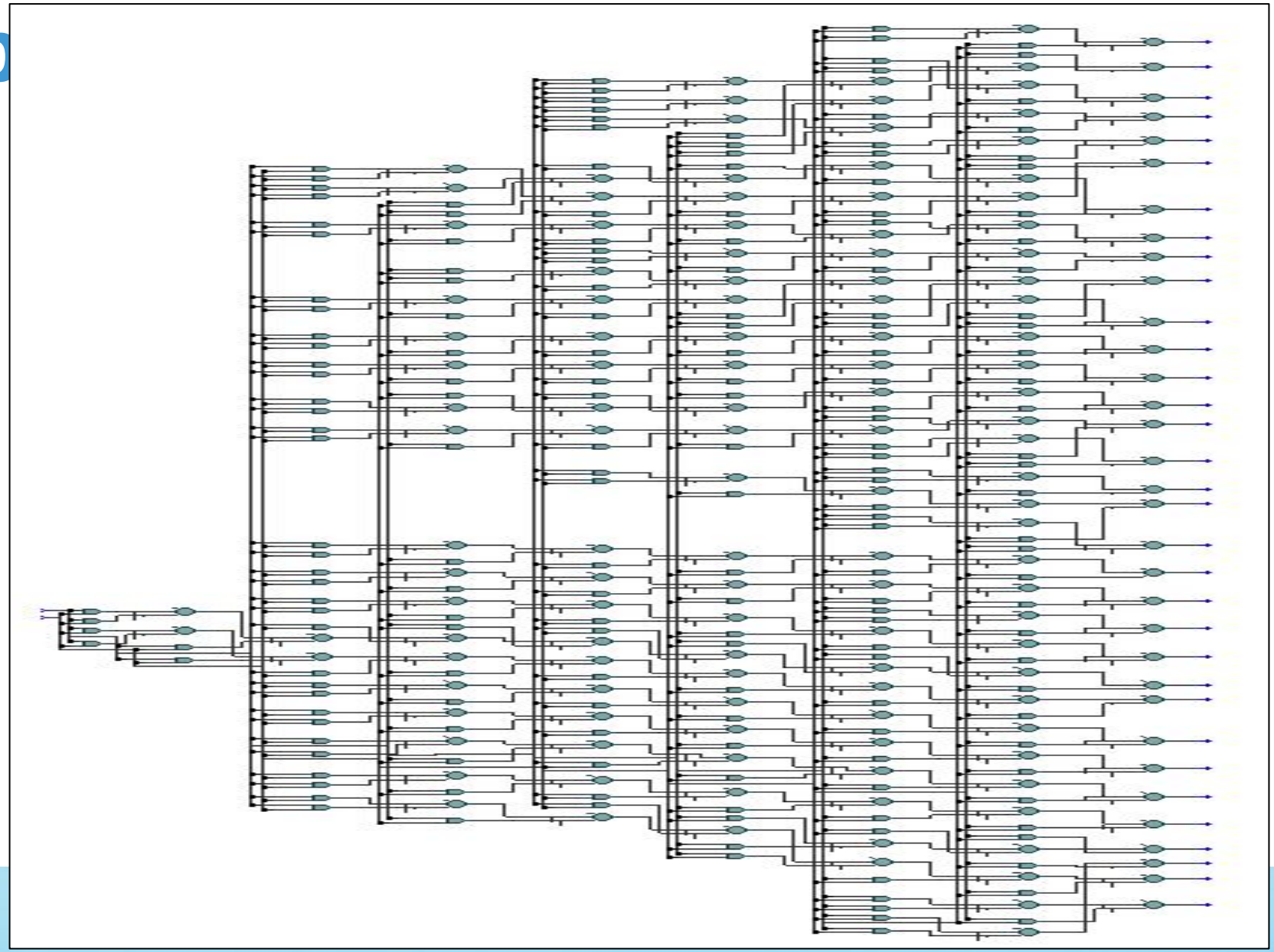
Example No. 1

```
adder[0] = 0010011011000100( 9924)
adder[1] = 0010011011010100( 9940)
adder[2] = 0001011010110010( 5810)
p = 20022 q = 19020
Product = 00001011010110010110101000000001000(380818440)
```

Example No. 2

```
adder[0] = 0111010101110100(30068)
adder[1] = 0111010111000001(30145)
adder[2] = 0001111000110101( 7733)
p = 28765 q = 17620
Product = 00001111000110101110000010000010O(506839300)
```

Register Transfer level of 64-bit Vedic Multip



Evidence

Parameter	Booth encoded parallel multiplier	Modified Booth Encoding Multiplier	Vedic Multiplier
Gate Count	20557	17196	5753
Area (μm^2)	102183	85983	28765
Power (mW)	13.7	12.1	3.98

Comparison report of current design with different Standard multiplier

Application of Vedic Multiplier

1. Digital signal processing: The Vedic multiplier can be used in digital signal processing applications to perform fast and accurate multiplication of two numbers.
2. Image processing: In image processing applications, the Vedic multiplier can be used to perform multiplication operations on large sets of data.
3. Cryptography: The Vedic multiplier can be used in cryptographic applications that require fast and secure multiplication operations.
4. High-performance computing: The Vedic multiplier can be used in high-performance computing applications that require fast and efficient multiplication operations.
5. Communication systems: The Vedic multiplier can be used in communication systems for performing multiplication operations on large data sets.

Conclusion

- The novelty of this proposed architecture is the reduction of power, delay and area in the prefix computation stages in Power Ground (PG) logic and bit-addition logic that leads to an overall reduction in area-delay product (ADP) and power-delay product (PDP).
- From the physical synthesis results, this is clear that the proposed Vedic multiplier architecture is 3 times more efficient than the next corresponding Booth architecture.
- Adding to it Vedic Multiplication was comparatively better than other existing multiplication in better terms of the low power, smaller area and high speed(lesser delay).

Summary

- The architecture of a Vedic Multiplier has fewer steps and use of simpler components resulting in a lesser bill of materials and a smaller footprint
- This results in lower propagation delays, lower power, reduced timing and lesser area than existing 64-bit multipliers .
- This algorithm is for a fundamental design component and has potentials to disrupt current library component usage as well as be a building block for future designs for ASICs and DSPs.